

DATA SHEET

74ABT16823A

74ABTH16823A

18-bit bus interface D-type flip-flop
with reset and enable (3-State)

Product specification
Supersedes data of 1995 Sep 28
IC23 Data Handbook

1998 Feb 27

18-bit bus-interface D-type flip-flop with reset and enable (3-State)

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74ABTH16823A

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16823A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up Reset
- Output capability: +64mA/−32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16823A 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT16823A has two 9-bit wide buffered registers with Clock Enable (\overline{nCE}) and Master Reset (\overline{nMR}) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

Two options are available, 74ABT16823A which does not have the bus-hold feature and 74ABTH16823A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	2.3 1.9	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_O = 0\text{V}$ or V_{CC} ; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	μA
I_{CCL}		Outputs low; $V_{CC} = 5.5\text{V}$	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	−40°C to +85°C	74ABT16823A DL	BT16823A DL	SOT371-1
56-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABT16823A DGG	BT16823A DGG	SOT364-1
56-Pin Plastic SSOP Type III	−40°C to +85°C	74ABTH16823A DL	BH16823A DL	SOT371-1
56-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABTH16823A DGG	BH16823A DGG	SOT364-1

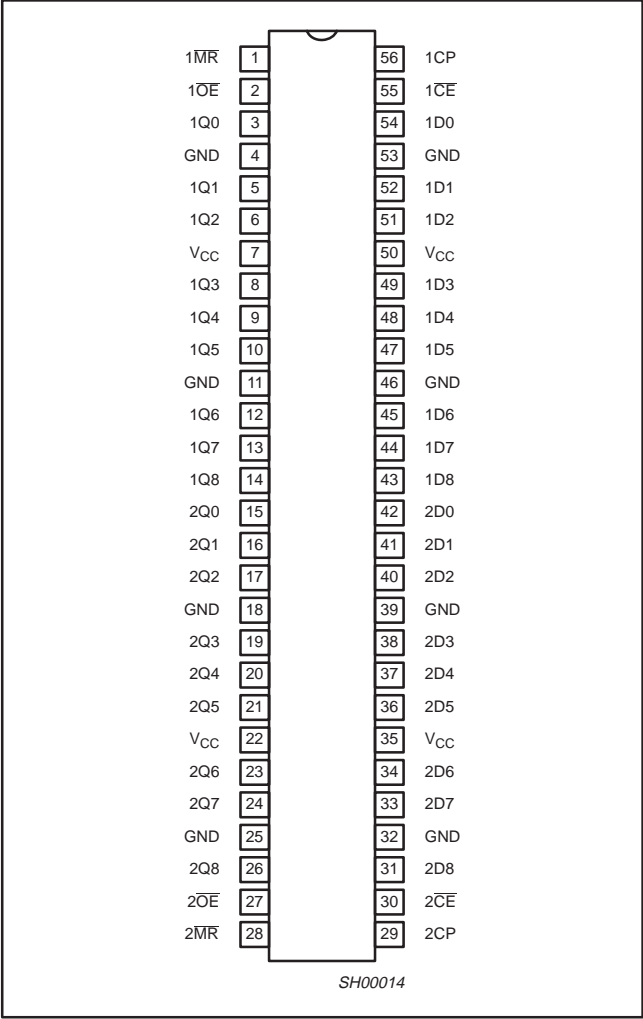
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 27	1OE, 2OE	Output enable input (active-Low)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	1D0-1D8 2D0-2D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	1Q0-1Q8 2Q0-2Q8	Data outputs
56, 29	1CP, 2CP	Clock pulse input (active rising edge)
55, 30	1CE, 2CE	Clock enable input (active-Low)
1, 28	1MR, 2MR	Master reset input (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

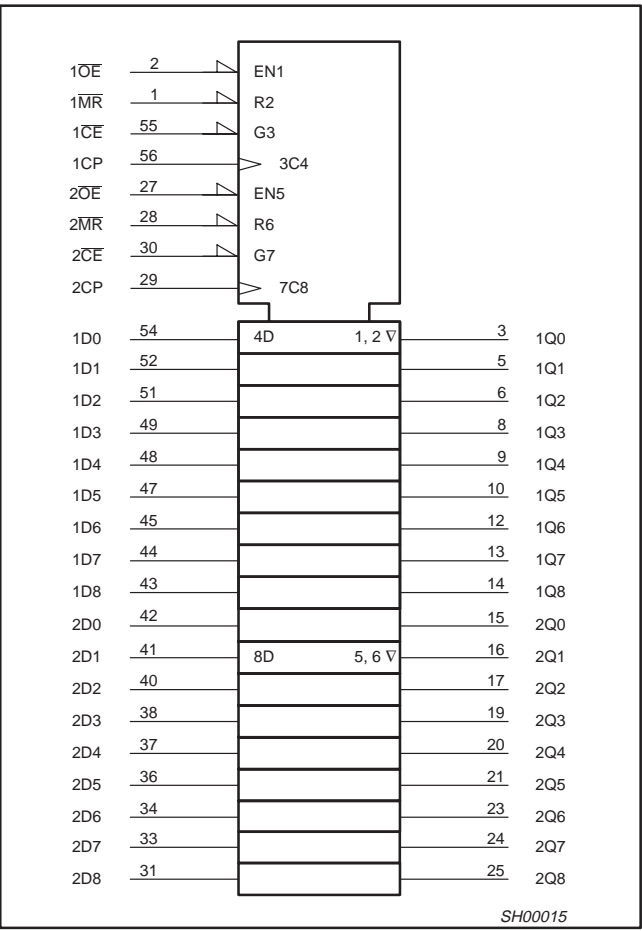
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PIN CONFIGURATION



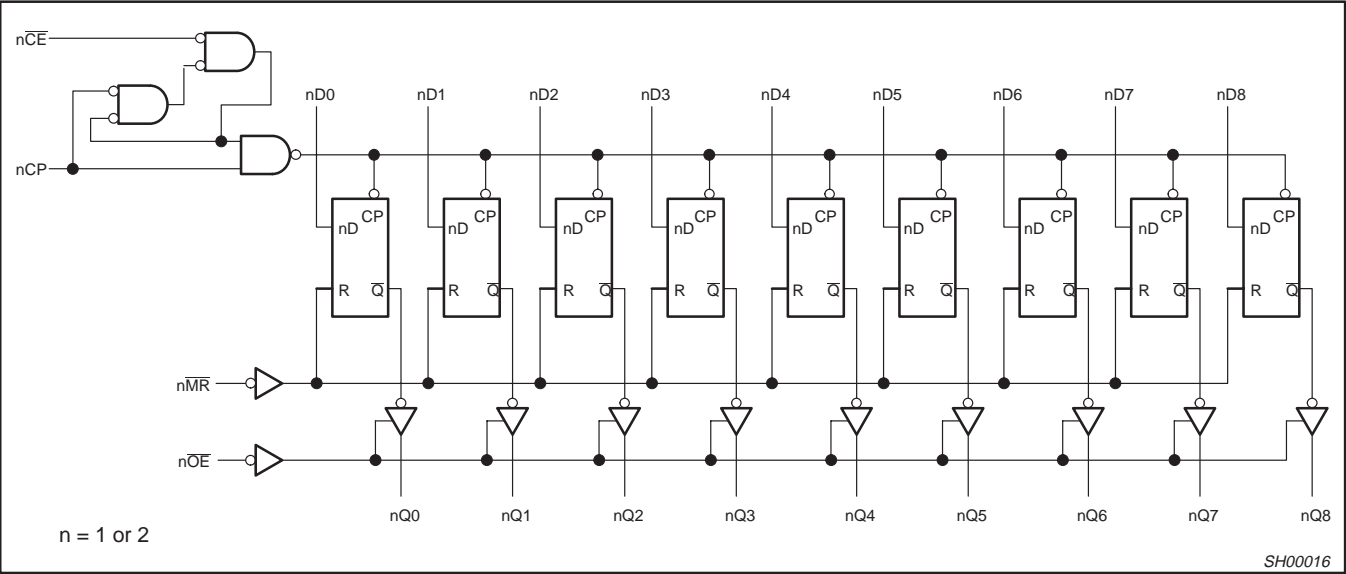
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
nOE	nMR	nCE	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	⊠	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
⊠ = Not a Low-to-High clock transition

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage ³		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA			-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}		2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}		3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}		2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}			0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³	V _{CC} = 5.5V; I _{OL} = 1mA; V _I = GND or V _{CC}			0.13	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = V _{CC} or GND			±0.01	±1		±1	μA
I _I	Input leakage current 74ABTH16823A	V _{CC} = 5.5V; V _I = V _{CC} or GND	Control pins		±0.01	±1		±1	μA
		V _{CC} = 5.5V; V _I = V _{CC}	Data pins		0.01	1		1	μA
		V _{CC} = 5.5V; V _I = 0			-2	-3		-5	μA
I _{HOLD}	Bus Hold current inputs ⁵ 74ABTH16823A	V _{CC} = 4.5V; V _I = 0.8V		35			35		μA
		V _{CC} = 4.5V; V _I = 2.0V		-75			-75		
		V _{CC} = 5.5V; V _I = 0 to 5.5V		±800					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V			±5.0	±100		±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} , V _{OE} = Don't care			±5.0	±50		±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}			1.0	10		10	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}			-1.0	-10		-10	μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}			50	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V		-50	-80	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}			0.5	1		1	mA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}			9.0	19		19	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}			0.5	1		1	mA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND			0.2	1		1	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100μsec is permitted.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

18-bit bus-interface D-type flip-flop with reset and enable (3-State)

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AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = −40°C to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	1	140	190		140		MHz
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	1	1.4 1.2	2.3 1.9	3.2 2.6	1.4 1.2	3.7 2.9	ns
t _{PHL}	Propagation delay nMR to nQx	2	2.0	3.3	4.3	2.0	5.0	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	4 5	1.3 1.2	2.4 2.1	3.2 2.9	1.3 1.2	3.9 3.4	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	4 5	1.7 1.6	2.9 2.3	4.0 3.2	1.7 1.6	4.7 3.4	ns

AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			MIN	TYP	MIN	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low nDx to nCP	3	2.0 1.5	1.3 0.9	2.0 1.5	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low nDx to nCP	3	1.5 1.5	-0.9 -1.2	1.5 1.5	ns
$t_w(\text{H})$ $t_w(\text{L})$	nCP pulse width High or Low	1	3.3 3.3	1.7 1.7	3.3 3.3	ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low nCE to nCP	3	1.5 2.0	0.9 0.9	1.5 2.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low nCE to nCP	3	1.5 1.5	-0.8 -0.9	1.5 1.5	ns
$t_w(\text{L})$	nMR pulse width, Low	2	3.0	1.7	3.0	ns
t_{rec}	Recovery time nMR to nCP	2	2.5	1.0	2.5	ns

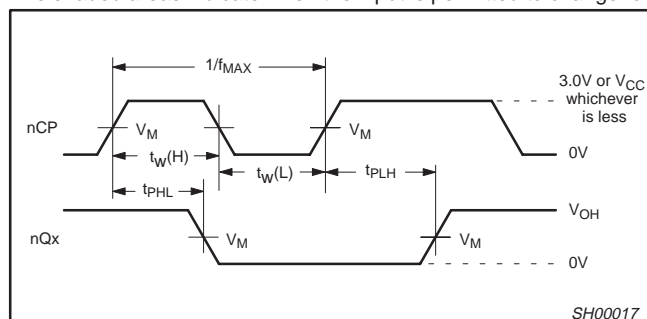
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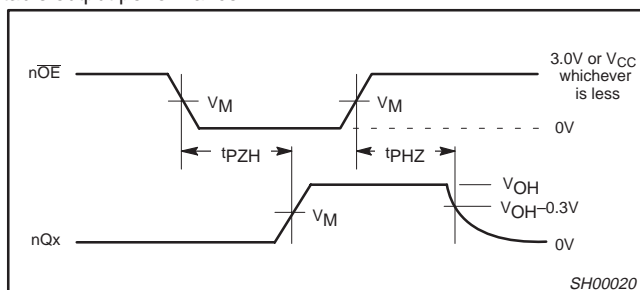
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

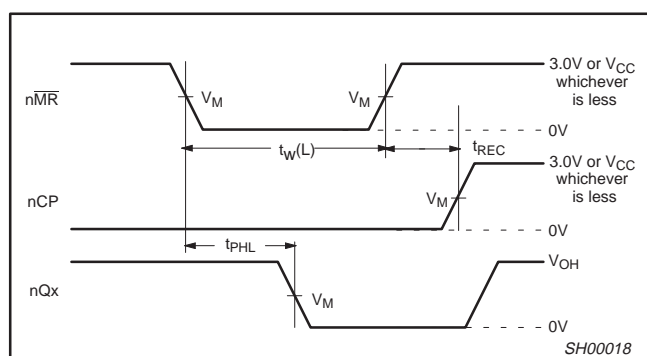
The shaded areas indicate when the input is permitted to change for predictable output performance.



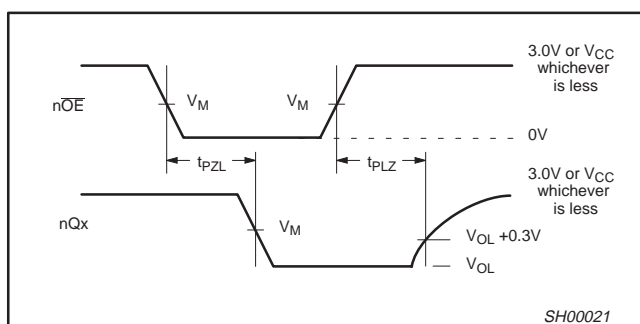
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



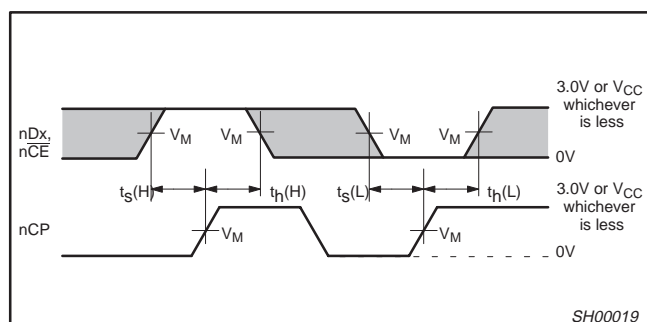
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

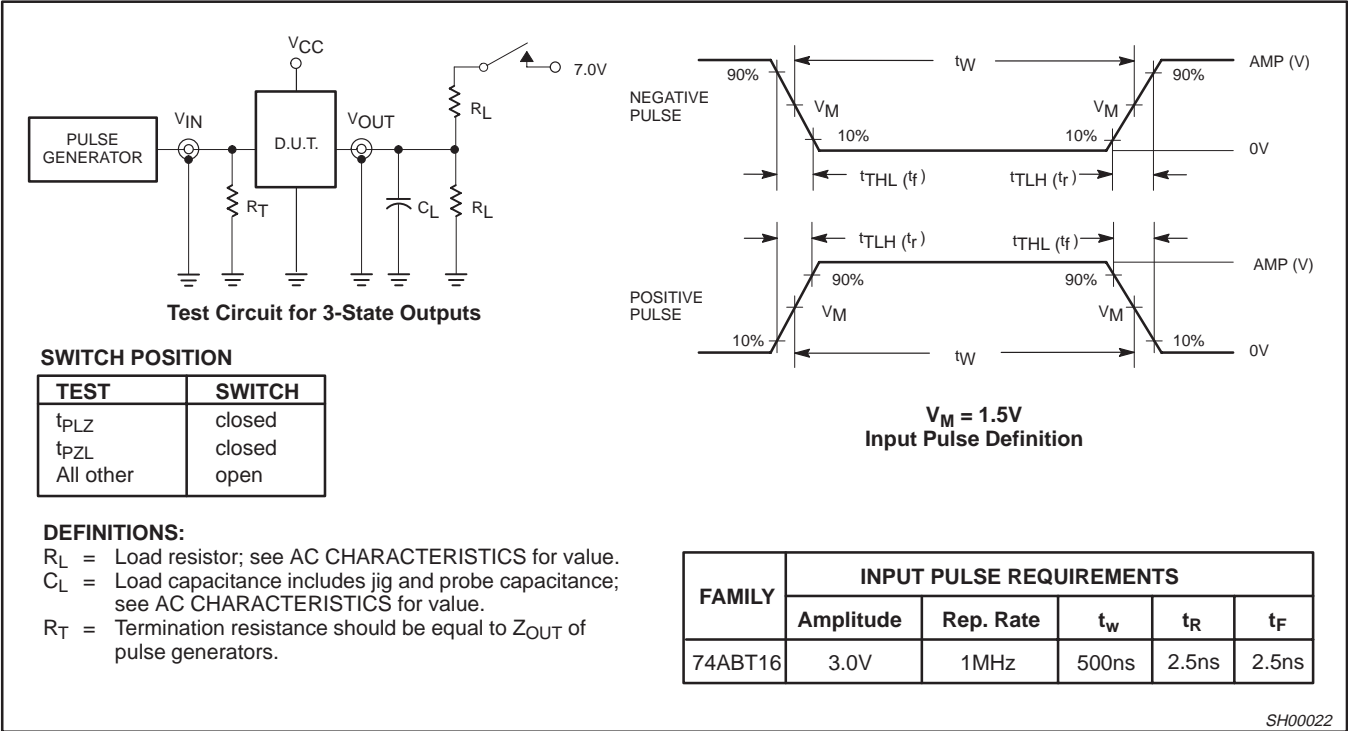


Waveform 3. Data Setup and Hold Times

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TEST CIRCUIT AND WAVEFORM

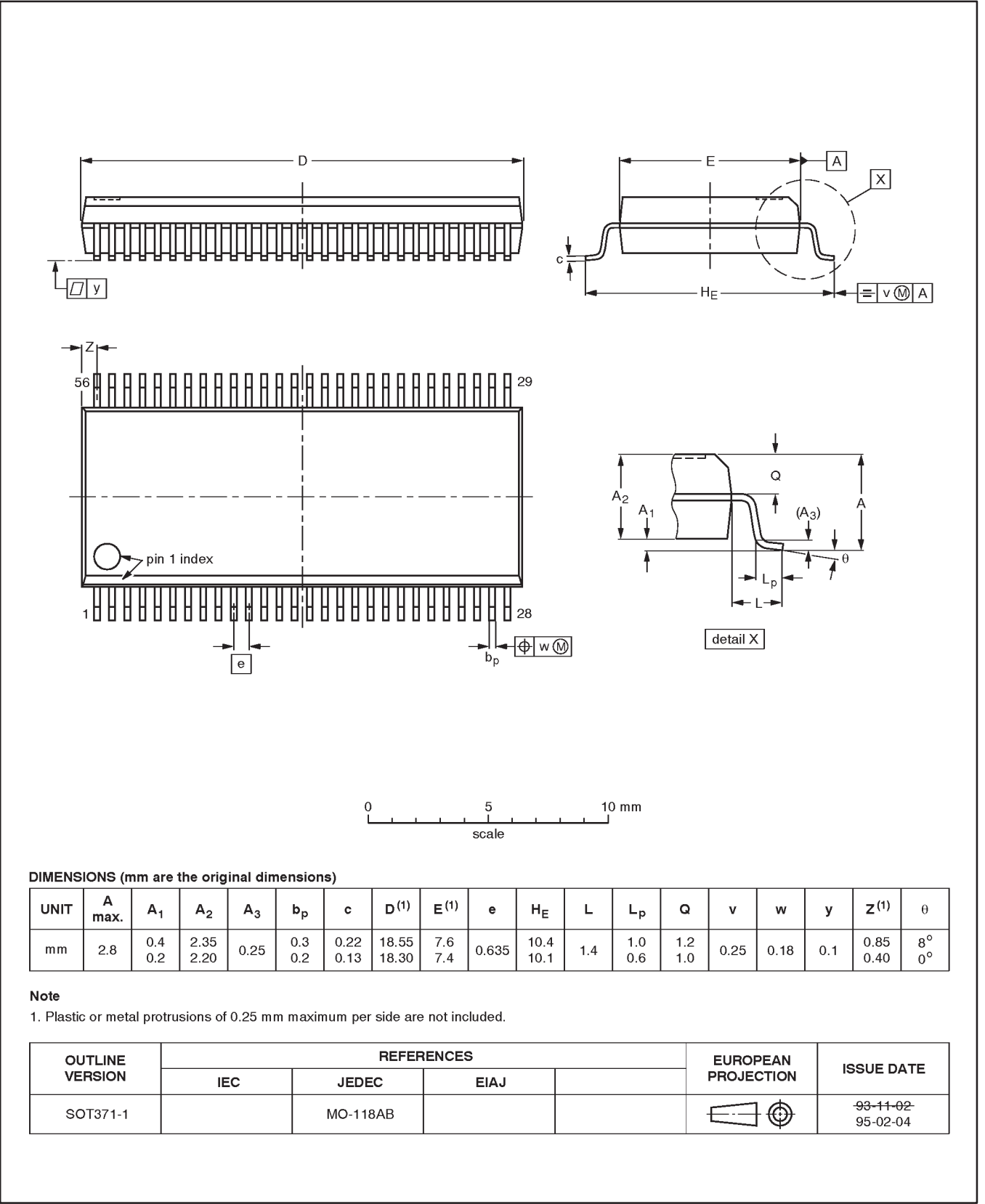


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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

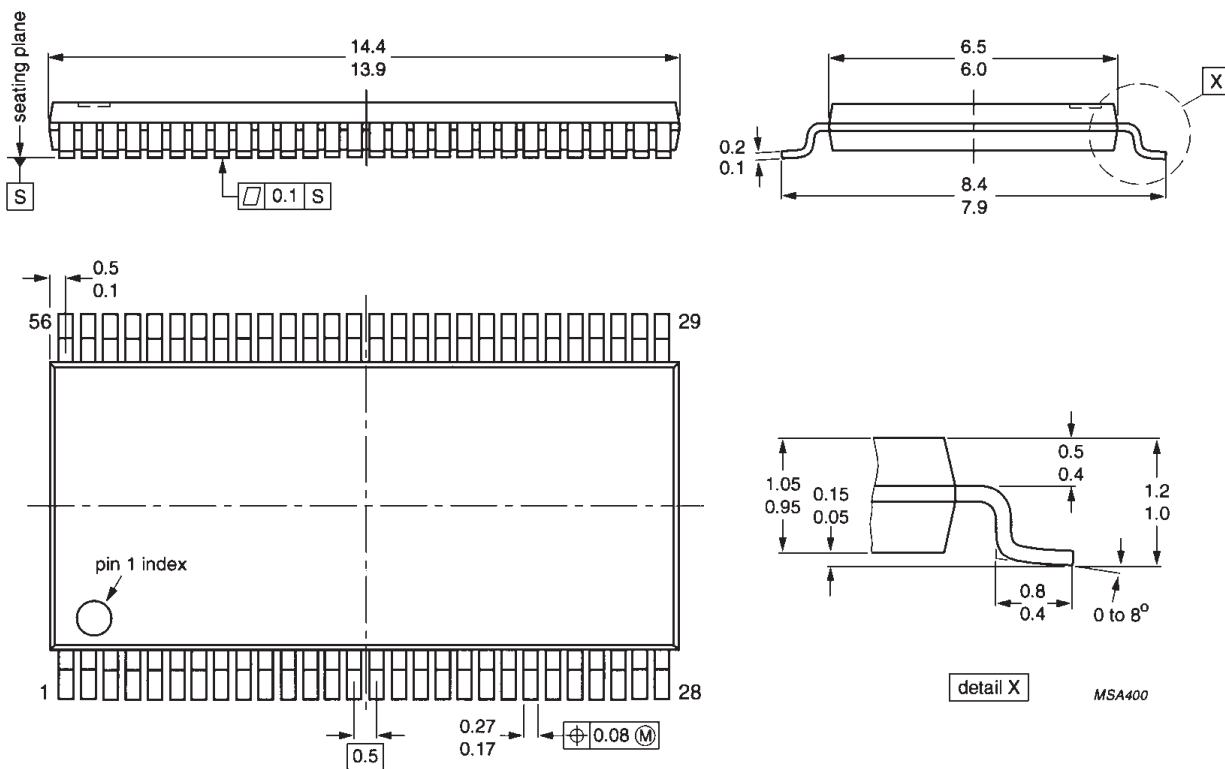


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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



18-bit bus-interface D-type flip-flop with reset and enable (3-State)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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